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AUSTRALIAN COMMUNICATIONS INDUSTRY FORUM

Australian Standard

Requirements for Customer Equipment for connection to hierarchical digital interfaces

Australian Communications Authority

Standards Australia

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FOREWORD

General

This Standard was prepared by the ACIF Working Committee CECRP/WC6 on Digital Standards for Customer Equipment. It is one of a series of Telecommunication Standards developed under the Memorandum of Understanding between the Australian Communications Authority and the Australian Communications Industry Forum.

This Standard is the result of a consensus among representatives on the ACIF Working Committee to produce it as an Australian Standard.

This Standard is based on the Australian Communications Authority ACA TS 016 — 1997 *Requirements For Customer Equipment For Connection To Hierarchical Digital Interfaces*.

The requirements in this Standard are consistent with the aims of s376 of the *Telecommunications Act 1997*. Specifically these aims are—

(a) protecting the integrity of a telecommunications network or facility;

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(d) ensuring interoperability with a standard telephone service.

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PARTICIPANTS

The ACIF Working Committee that developed this standard consisted of the following organisations:

Organisation	Membership
Australian Communications Authority	Non-voting
Australian Communications Industry Forum	Non-voting
Australian Telecommunications Industry Association	Voting
Comtest Laboratories	Voting
Envision Communications	Voting
Lucent Techologies	Voting
NEC Australia	Voting
Siemens	Voting
Telstra	Voting

1 INTERPRETATION

1.1 Categories of requirements

This Standard contains mandatory requirements as well as provisions that are recommendations only. Mandatory requirements are designated by the words '**shall**' or '**shall not**'. All other provisions are voluntary.

1.2 Compliance statements

Compliance statements, in italics, suggest methodologies for demonstrating CE's compliance with the requirements

1.3 Definitions, expressions and terms

If there is any conflict between the definitions used in this Standard and the definitions used in the *Telecommunications Act 1997*, the definitions in the *Act* take precedence.

1.4 Notes

Text denoted as 'Note' is for guidance in interpretation and is shown in smaller size type.

1.5 Categories of requirements

1.5.1 Applicable editions (or versions) of other documents referred to in this Standard are referenced documents and are specified in Section 3: REFERENCES.

1.5.2 If a document refers to another document, the other document is a sub-referenced document.

1.5.3 Where the edition (or version) of the sub-referenced document is uniquely identified in the reference document, then that edition (or version) applies.

1.5.4 Where the edition (or version) of the sub-referenced document is not uniquely identified in the reference document, then the applicable edition (or version) of a legislated document is that which is current at the date the reference document is legislated under the applicable regulatory framework or otherwise comes into effect, or for a non-legislated document, the date upon which the document is published by the relevant standards organisation.

1.5.5 A number in square brackets '[ ]' refers to a document listed in Section 3: REFERENCES.

1.5.6 In the event of a discrepancy between this Standard and a referenced or sub-referenced document, this Standard **shall** take precedence.

1.6 Units and symbols

In this Standard the International System (SI) of units and symbols is used in accordance with Australian Standard AS ISO 1000 [1].

2 SCOPE

2.1 This Standard applies to Customer Equipment with hierarchical digital interfaces at 2048 kbit/s, 8448 kbit/s, 34 368 kbit/s or 139 264 kbit/s that is designed or intended for connection to a Telecommunications Network.

2.2 The CE-Network requirements in this Standard describe a point-to-point configuration as shown in Figure 1. This configuration comprises two connections, one for digital transmission from the CE to Network and one for digital transmission from the Network to CE.

Note 1: Point-to-point configuration at Layer 1 implies that for each direction only one source (transmitter) and one sink (receiver) are connected to the interface. The maximum reach of the interface in the point-to-point configuration is limited by the specification for the electrical characteristics of transmitted and received pulses and the type of interconnecting cable.

Note 2: The use of HDB3 or CMI (refer to Figure 2) coding removes the need to provide separate synchronisation connections.

2.3 CE is not excluded from the scope of this Standard by reason only that it is capable of performing functions additional to those listed herein.

3 REFERENCES

	Australian Standards	
[1]	AS ISO 1000-1998	The International System of Units (SI) and its application
[2]	AS/NZS 60950:2000	Safety of information technology equipment (IEC 60950:1999, MOD)
	ITU–T Recommendations	
[3]	G.703:1998	Physical/electrical characteristics of hierarchical digital interfaces
[4]	G.823:2000	The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy
[5]	O.151:1992	Error performance measuring equipment for digital systems at the primary rate and above
	IEC International Standards	
[6]	IEC 60950:1999	Safety of information technology equipment

4 ABBREVIATIONS AND DEFINITIONS

For the purposes of this Standard, the following abbreviations and definitions apply.

4.1 Abbreviations

ppm	Parts per Million
AC	Alternating Current
ACA	Australian Communications Authority
ACIF	Australian Communications Industry Forum
AIS	Alarm Indication Signal
AMI	Alternate Mark Inversion Code
AS	Australian Standard
BER	Bit Error Rate
CE	Customer Equipment
CMI	Coded Mark Inversion Code
CRC	Cyclic Redundancy Check
CRO	Cathode Ray Oscilloscope
DC	Direct Current
EMC	Electromagnetic Compatibility
FAS	Frame Alignment Signal
HDB3	High Density Bipolar code of order 3
HF	High Frequency
IEC	International Electrotechnology Commission
ISO	International Standardization Organization
ITU-T	International Telecommunication Union - Telecommunication Standardization Sector
NZS	New Zealand Standard
PRBS	Pseudo Random Binary Sequence
SELV	Safety Extra Low Voltage
SI	International System
SMF	Sub Multiframe
TNV	Telecommunications Network Voltage
UI	Unit Interval

4.2 Definitions

4.2.1 Carrier

Refer to Section 7 of the *Telecommunications Act 1997*.

4.2.2 Customer Equipment

Refer to Section 21 of the *Telecommunications Act 1997*.

4.2.3 Facility

Refer to Sub-section 374(2) of the *Telecommunications Act 1997*.

4.2.4 Intrinsic Jitter

Intrinsic jitter is the jitter present at the output port of equipment when it is receiving no jitter at its input, or when receiving no input signal.

4.2.5 Safety Extra Low Voltage (SELV)

Refer to AS/NZS 60950:2000 [2]

4.2.6 Telecommunications Network

Refer to sub-section 374(1) of the *Telecommunications Act 1997*.

4.2.7 Unit Interval

The nominal difference in time between consecutive significant instants of an isochronous signal.

5 REQUIREMENTS

5.1 General

5.1.1 Fail-safe operation

5.1.1.1 CE **shall not** cause harm or damage to a Telecommunications Network or Facility if any of the following events occur:

(a) Failure of any mechanical or electrical component in the CE.

(b) Failure of any power supplies, resulting in total or partial loss of power, to the CE.

(c) Discharge or partial discharge of any battery supply.

(d) Incorrect manual operation of the CE.

5.1.1.2 CE should not cause harm or damage to a Telecommunications Network or Facility when CE is operated outside the range of operating voltage and environmental conditions specified by the manufacturer.

Compliance with Clause 5.1.1 should be checked by operation and inspection

5.1.2 Line polarity and line conductor polarisation

The operation of the CE should be independent of—

(a) line conductor polarisation for balanced pair interfaces, i.e. the connection of specific conductors of the line pair to specific line terminals of the CE; and

(b) the polarity of any voltage on any specific line conductor.

Compliance with Clause 5.1.2 should be checked by operation and inspection.

5.1.3 Interface

5.1.3.1 Port rating label

Where a port is only designed for connection to an SELV service, it **shall** be identified by a label attached to the CE.

Compliance with Clause 5.1.3.1 should be checked by inspection.

5.1.3.2 DC line potential

The operation of CE intended or designed for connection to a Telecommunications Network service **shall not**—

(a) require provision of a DC potential from the Telecommunications Network; or

(b) apply a DC potential to the Telecommunications Network.

Compliance with Clause 5.1.3.2 should be checked by operation and inspection.

5.2 Configuration

5.2.1 Timing functions

5.2.1.1 The CE **shall** provide an interface on which the information and timing signal are in the same direction, i.e. co-directional.

5.2.1.2 A CE **shall** be capable of synchronising its timing to the signal received from the Telecommunications Network.

5.2.1.3 The CE **shall** be capable of synchronising its transmitted signal to a timing signal received from the Telecommunications Network.

5.2.1.4 If a CE cannot synchronise with a Telecommunications Network due to, for example, loss of received signal or reception of AIS, the CE **shall** transmit using an internal clock complying with the relevant requirements of Clauses 5.3, 5.4, 5.5, or 5.6.

Note : If the CE receives more than one signal from the network, timing is usually derived from any one of these inputs. The CE should select as its current synchronisation source a network signal input which is not experiencing loss of signal, loss of synchronisation, or reception of AIS (see Clause 5.2.3)

Compliance with Clause 5.2.1 should be checked using the methods as described in Clause 6.3

5.2.2 Earthing of outer conductor or screen

5.2.2.1 Where the CE is designed to connect to a Telecommunications Network using a co-axial cable or screened balanced pair cable, the output port of the CE **shall** provide a means to connect the outer conductor of the co-axial connector or the screen of the balanced pair connector to the protective earth terminal.

5.2.2.2 Where the CE is designed to connect to a Telecommunications Network using a co-axial cable or screened balanced pair cable, the input port of the CE should provide a means of connecting/disconnecting the outer conductor of the co-axial connector or the screen of the balanced pair connector to the protective earth terminal.

Note 1: Clause 5.2.2.2 allows for either a connection to protective earth at the input port as required by ITU-T Rec. G.703 [3] or allows for provision to connect and disconnect the co-axial cable outer conductor or balanced pair cable screen to protective earth at the input port of the CE.

Note 2: Care needs to be exercised in earthing practice as most existing network side equipment provides a solid earth at both input and output ports.

Note 3: The direct connection of the outer conductors of co-axial cables to the protective earth at the transmit and receive interfaces may, because of differences in earth potential at each end of the cable, result in unwanted current flowing in the outer conductor, through connectors and through the receiver input circuitry. This may result in errors or even permanent damage. To prevent this problem, DC isolation may be introduced between the outer conductor and protective earth at the receive interface.

Note 4: Clause 5.2.2 does not apply to CE designed to connect to a Telecommunications Network using an unscreened balanced pair cable.

Compliance with Clause 5.2.2 should be checked by inspection.

5.2.3 Alarm Indication Signal (AIS)

5.2.3.1 AIS detection is based on the assumption that the received signal has fewer zeros (0s) than a signal consisting of all ones (1s) with a valid Frame Alignment Signal (FAS) for a given bit rate.

5.2.3.2 Under normal operating conditions, a transmitted signal from the CE should avoid simulating AIS.

Note: AIS is an unframed signal used by carriers to trace service faults. This signal consists of continuous ones (1s) on the line, which may be injected by equipment when loss of incoming signal, loss of synchronisation or high error rate is detected.

The signal causes AIS Indicators to activate on equipment receiving it, raising non-urgent network alarms, and aids rapid restoration of service by indicating that a fault exists elsewhere on the link.

Some CE generates signals that simulate AIS when no fault exists. This may lead to manual disabling of network alarms, and to delays in service restoration for this type of CE. Use of data scrambling or framing, which meets the above criterion, will generally avoid AIS simulation.

5.2.3.3 An all ones (1s) condition may also exist within a single time slot of a received signal. If this condition should occur, the CE should not respond to the condition as an AIS.

Compliance with Clause 5.2.3 should be checked using the methods as described in Clause 6.7.

5.3 2048 kbit/s

5.3.1 Interfaces

The CE interface **shall** provide a 75 Ω coaxial and/or a 120 Ω balanced (symmetrical pair) connection.

Compliance with Clause 5.3.1 should be checked by inspection.

5.3.2 Bit rates

The 2048 kbit/s interface **shall** operate at 2048 kbit/s ±50 ppm.

Compliance with Clause 5.3.2 should be checked using the methods as described in Clause 6.3.

5.3.3 Line coding

The CE **shall** be capable of receiving and transmitting High Density Bipolar code of order 3 (HDB3) coding in accordance with Annex A of ITU–T Rec. G.703 [3].

Compliance with Clause 5.3.3 should be checked using the methods as described in Clause 6.4.

5.3.4 Output signal pulse shape

5.3.4.1 75 Ω interface mark

The pulse shape at the output port terminated with a 75 Ω resistor **shall** conform with the mask in Figure 3, where the nominal pulse height is 2.37 V.

5.3.4.2 120 Ω interface mark

The pulse shape at the output port terminated with a 120 Ω resistor **shall** conform with the mask in Figure 3, where the nominal pulse height is 3.0 V.

5.3.4.3 Space

The height limit of a space (no-pulse) at the output port terminated with a resistor of the nominal port impedance **shall** be 0 V ±10% of the nominal pulse height.

Note: The loading of an input port can distort the output pulse sufficiently so that it no longer matches the pulse mask. Output ports should be tested for this source of distortion. Also refer Appendix A

Compliance with Clause 5.3.4 should be checked using the methods as described in Clause 6.8.

5.3.5 Input port

5.3.5.1 Return loss

The return loss of a 2048 kbit/s input port against a resistor of the nominal port impedance of the port **shall** have the minimum values listed in Table 1.

TABLE 1

Return loss requirements 2048 kbit/s

Frequency range (kHz)			Return loss (dB)
51	to	102	12
102	to	2048	18
2048	to	3072	14

Compliance with Clause 5.3.5.1 should be checked using the methods as described in Clause 6.9.

5.3.5.2 Sensitivity

The CE **shall** operate without errors, when the input port is connected to a source in accordance with Clause 5.3.4, modified with an interconnecting cable attenuation of 0 dB to 6 dB measured at 1024 kHz with an attenuation slope proportional to the square root of frequency.

Compliance with Clause 5.3.5.2 should be checked using the methods as described in Clause 6.10.

5.3.5.3 Immunity

To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, a combined signal, attenuated up to the maximum specified interconnecting cable attenuation (Clause 5.3.5.2), applied to the input port, **shall not** result in errors.

To generate the combined signal, the wanted signal which complies with Clauses 5.3.1 to 5.3.4 is added to an interfering signal with the following characteristic:

(a) With the same pulse shape as the wanted signal.

(b) With a bit rate within the limits set out in the standard.

(c) Not synchronous with the wanted signal.

(d) Combined with the wanted signal in a combining network.

(e) With an overall zero loss in the wanted signal's path.

(f) With a nominal impedance of—

  (i) 75 Ω for a coaxial-pair interface; or

  (ii) 120 Ω for a symmetrical-pair interface.

(g) With a signal-to-interference ratio of 18 dB.

(h) With a binary content that complies with ITU–T Rec. O.151 [5] (2^{15}–1 bit pattern).

Note : It is recommended to use a receiver implementation that provides an adaptive threshold rather than one that provides a fixed threshold. An adaptive threshold should be less susceptible to errors due to reflections.

Compliance with Clause 5.3.5.3 should be checked using the methods as described in Clause 6.11.

5.3.6 Intrinsic jitter

The intrinsic jitter present at the output port of the CE **shall not** exceed the values in Figure 8.

Compliance with Clause 5.3.6 should be checked using the methods as described in Clause 6.5.

5.3.7 Input jitter and wander tolerance

CE **shall** operate without degradation of performance when receiving signals modulated with sinusoidal jitter up to the limit shown in Figure 9.

Compliance with Clause 5.3.7 should be checked using the methods as described in Clause 6.6.

5.4 8448 kbit/s

5.4.1 Interfaces

The CE interface **shall** provide a 75 Ω coaxial connection.

Compliance with Clause 5.4.1 should be checked by inspection

5.4.2 Bit rates

The 8448 kbit/s interface **shall** operate at 8448 kbit/s ± 30 ppm.

Compliance with Clause 5.4.2 should be checked using the methods as described in Clause 6.3.

5.4.3 Line coding

The CE **shall** be capable of receiving and transmitting High Density Bipolar code of order 3 (HDB3) coding in accordance with Annex A of ITU–T Rec. G.703 [3].

Compliance with Clause 5.4.3 should be checked using the methods as described in Clause 6.4.

5.4.4 Output signal pulse shape

5.4.4.1 Mark

The pulse shape at the output port terminated with a 75 Ω resistor **shall** conform with the mask in Figure 4, where the nominal pulse height is 2.37 V.

5.4.4.2 Space

The height limit of a space (no pulse) at the output port terminated with a 75 Ω resistor **shall** be 0 V ± 0.237 V.

Compliance with Clause 5.4.4 should be checked using the methods as described in Clause 6.8.

5.4.5 Input Port

5.4.5.1 Return loss

The return loss of an 8448 kbit/s input port against a 75 Ω resistive load **shall** have the minimum values listed in Table 2.

TABLE 2

Return loss requirements 8448 kbit/s

Frequency range (kHz)			Return loss (dB)
211	to	422	12
422	to	8448	18
8448	to	12 672	14

Compliance with Clause 5.4.5.1 should be checked using the methods as described in Clause 6.9.

5.4.5.2 Sensitivity

The CE **shall** operate without errors, when the input port is connected to a source in accordance with Clause 5.4.4, modified with an interconnecting cable attenuation of 0 dB to 6 dB measured at 4224 kHz with an attenuation slope proportional to the square root of frequency.

Compliance with Clause 5.4.5.2 should be checked using the methods as described in Clause 6.10.

5.4.5.3 Immunity

To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, a combined signal, attenuated up to the maximum specified interconnecting cable attenuation (Clause 5.4.5.2), applied to the input port, **shall not** result in errors.

To generate the combined signal, the wanted signal which complies with Clauses 5.4.1 to 5.4.4 is added to an interfering signal with the following characteristic:

(a) With the same pulse shape as the wanted signal.

(b) With a bit rate within the limits set out in the standard.

(c) Not synchronous with the wanted signal.

(d) Combined with the wanted signal in a combining network.

(e) With an overall zero loss in the wanted signal path.

(f) With a nominal impedance of 75 Ω for a coaxial-pair interface.

(g) With a signal-to-interference ratio of 20 dB.

(h) With a binary content that complies with ITU–T Rec. O.151 [5] (2^{15}–1 bit pattern).

Compliance with Clause 5.4.5.3 should be checked using the methods as described in Clause 6.11.

5.4.6 Intrinsic jitter

The intrinsic jitter present at the output port of the CE **shall not** exceed the values in Figure 8.

Compliance with Clause 5.4.6 should be checked using the methods as described in Clause 6.5.

5.4.7 Input jitter and wander tolerance

The CE interface **shall** operate without degradation of performance when receiving signals modulated with sinusoidal jitter up to the limit shown in Figure 9.

Compliance with Clause 5.4.7 should be checked using the methods as described in Clause 6.6.

5.5 34 368 kbit/s

5.5.1 Interfaces

The CE interface **shall** provide a 75 Ω coaxial connection.

Compliance with Clause 5.5.1 should be checked by inspection

5.5.2 Bit rates

The 34 368 kbit/s interface **shall** operate at 34 368 kbit/s ±20 ppm.

Compliance with Clause 5.5.2 should be checked using the methods as described in Clause 6.3.

5.5.3 Line coding

The CE **shall** be capable of receiving and transmitting High Density Bipolar code of order 3 (HDB3) coding in accordance with Annex A of ITU–T Rec. G.703 [3].

Compliance with Clause 5.5.3 should be checked using the methods as described in Clause 6.4.

5.5.4 Output signal pulse shape

5.5.4.1 Mark

The pulse shape at the output port terminated with a 75 Ω resistor **shall** conform with the mask in Figure 5, where the nominal pulse height is 1.00 V.

5.5.4.2 Space

The height limit of a space (no-pulse) at the output port terminated with a 75 Ω resistor **shall** be 0 V ±0.100 V.

Compliance with Clause 5.5.4 should be checked using the methods as described in Clause 6.8.

5.5.5 Input port

5.5.5.1 Return loss

The return loss of a 34 368 kbit/s input port against a 75 Ω resistive load **shall** have the minimum values listed in Table 3.

TABLE 3

Return loss requirements 34 368 kbit/s

Frequency range (kHz)			Return loss (dB)
860	to	1720	12
1720	to	34 368	18
34 368	to	51 550	14

Compliance with Clause 5.5.5.1 should be checked using the methods as described in Clause 6.9.

5.5.5.2 Sensitivity

The CE **shall** operate without errors, when the input port is connected to a source in accordance with Clause 5.5.4, modified with an interconnecting cable attenuation of 0 dB to 12 dB measured at 17 184 kHz with an attenuation slope proportional to the square root of frequency.

Compliance with Clause 5.5.5.2 should be checked using the methods as described in Clause 6.10.

5.5.5.3 Immunity

To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, a combined signal, attenuated up to the maximum specified interconnecting cable attenuation (Clause 5.5.5.2), applied to the input port, **shall not** result in errors.

To generate the combined signal, the wanted signal which complies with Clauses 5.5.1 to 5.5.4 is added to an interfering signal with the following characteristic:

(a) With the same pulse shape as the wanted signal.

(b) With a bit rate within the limits set out in the standard.

(c) Not synchronous with the wanted signal.

(d) Combined with the wanted signal in a combining network.

(e) With an overall zero loss in the wanted signal path.

(f) With a nominal impedance of 75 Ω for a coaxial-pair interface.

(g) With a signal-to-interference ratio of 20 dB.

(h) With a binary content that complies with ITU–T Rec. O.151 [5] (2^{23}–1 bit pattern).

Compliance with Clause 5.5.5.3 should be checked using the methods as described in Clause 6.11.

5.5.6 Intrinsic jitter

The intrinsic jitter present at the output port of the CE **shall not** exceed the values in Figure 8.

Compliance with Clause 5.5.6 should be checked using the methods as described in Clause 6.5.

5.5.7 Input jitter and wander tolerance

Equipment **shall** operate without degradation of performance when receiving signals modulated with sinusoidal jitter up to the limit shown in Figure 9.

Compliance with Clause 5.5.7 should be checked using the methods as described in Clause 6.6.

5.6 139 264 kbit/s

5.6.1 Interfaces

The CE interface **shall** provide a 75 Ω coaxial connection.

Compliance with Clause 5.6.1 should be checked by inspection.

5.6.2 Bit rates

The 139 264 kbit/s interface **shall** operate at 139 264 kbit/s ±15 ppm.

Compliance with Clause 5.6.2 should be checked using the methods as described in Clause 6.3.

5.6.3 Line coding

The CE **shall** be capable of receiving and transmitting Coded Mark Inversion (CMI) line coding in accordance with Annex A of ITU–T Rec. G.703 [3].

Note: An illustration of CMI Coding Rules is given in Figure 2 (informative).

Compliance with Clause 5.6.3 should be checked using the methods as described in Clause 6.4.

5.6.4 Output port

5.6.4.1 Pulse shape: Binary 0

The pulse shape corresponding to a binary 0 at the output port terminated with a 75 Ω resistor **shall** conform with the mask of Figure 6.

Compliance with Clause 5.6.4.1 should be checked using the methods as described in Clause 6.8.

5.6.4.2 Pulse shape: Binary 1

The pulse shape corresponding to a binary 1 at the output port terminated with a 75 Ω resistor **shall** conform with the mask of Figure 7.

Compliance with Clause 5.6.4.2 should be checked using the methods as described in Clause 6.8.

5.6.4.3 Return loss

The return loss of a 139 264 kbit/s output port against a 75 Ω resistive load **shall** be 15 dB or greater for the frequency range 7 MHz to 210 MHz.

Compliance with Clause 5.6.4.3 should be checked using the methods as described in Clause 6.9.

5.6.5 Input port

5.6.5.1 Return loss

The return loss of a 139 264 kbit/s input port against a 75 Ω resistive load **shall** be 15 dB or greater for the frequency range 7 MHz to 210 MHz.

Compliance with Clause 5.6.5.1 should be checked using the methods as described in Clause 6.9.

5.6.5.2 Sensitivity

The CE **shall** operate without errors, when the input port is connected to a source in accordance with Clause 5.6.4, modified with an interconnecting cable attenuation of 0 dB to 12 dB measured at 70 MHz with an attenuation slope proportional to the square root of frequency.

Compliance with Clause 5.6.5.2 should be checked using the methods as described in Clause 6.10.

5.6.5.3 Intrinsic jitter

The intrinsic jitter present at the output port of the CE **shall not** exceed the values in Figure 8.

Compliance with Clause 5.6.7 should be checked using the methods as described in Clause 6.5.

5.6.6 Input jitter and wander tolerance

CE **shall** operate without degradation of performance when receiving signals modulated with sinusoidal jitter up to the limit shown in Figure 9.

Compliance with Clause 5.6.8 should be checked using the methods as described in Clause 6.6.

6 TESTING

6.1 General

6.1.1 Compliance with all mandatory requirements applicable to the CE as specified in the requirements clauses is to be verified. This verification may be through direct measurement, modelling and analysis, or inspection.

6.1.2 Methods for demonstrating compliance of CE with requirement clauses specified in this Standard are described in Clauses 6.2 to 6.11. Other methods may be used if the risk of passing non-compliant CE is not increased because of increased measurement uncertainty.

6.2 Standard test conditions

6.2.1 Conditions

Unless this Standard provides otherwise, testing for compliance with this Standard should be conducted at the nominal supply voltage of the CE and within the following ranges of atmospheric conditions:

(a) An ambient temperature in the range of 15°C to 25°C inclusive.

(b) A relative humidity in the range of 30% to 75% inclusive.

(c) An air pressure in the range of 86 kPa to 106 kPa inclusive.

6.2.2 Record keeping

The prevailing conditions should be recorded for each test.

6.3 Bit rate and tolerance test

6.3.1 Test specifications

The following Table lists the bit rate interfaces to be tested, together with a reference to the associated requirements clause, as applicable.

Interface (kbit/s)	Requirements Clause
2048	Clause 5.3.2
8448	Clause 5.4.2
34 368	Clause 5.5.2
139 264	Clause 5.6.2

6.3.2 Test method

The line bit rate at the output port should be measured using the test set-up of Figure 11.The clock signal extracted in the test set-up should be within the specified tolerances. This test should be carried out with the CE synchronised to its input signal for the full range of the appropriate bit rate specified and when free running.

6.4 Line coding rules

6.4.1 Test specifications

The following Table lists the bit rate interfaces to be tested, together with a reference to the associated requirements clause, as applicable.

Interface (kbit/s)	Requirements Clause
2048	Clause 5.3.3
8448	Clause 5.4.3
34 368	Clause 5.5.3
139 264	Clause 5.6.3

6.4.2 Test method

The line code should be measured using the test set-up of Figure 12. The CE should be made to transmit a PRBS for a period longer than a single cycle of the PRBS, to ensure that the coding rules are met. Using the test set-up, the output port should produce an output signal exhibiting the required coding.

6.5 Intrinsic jitter

6.5.1 Test specifications

The following Table lists the bit rate interfaces to be tested, together with a reference to the associated requirements clause, as applicable.

Interface (kbit/s)	Requirements Clause
2048	Clause 5.3.6
8448	Clause 5.4.6
34 368	Clause 5.5.6
139 264	Clause 5.6.6

6.5.2 Test method

The intrinsic jitter generated by the CE should be measured using the test set-up in Figure 14. The bit pattern generator should be set to the appropriate interface bit rate, and generate the recommended PRBS ($2^{15} - 1$ or $2^{23} - 1$).

With no input jitter, the measurement should be made with the cable loss set to 0 dB and to the maximum cable loss as specified in Clauses 5.3.5.2, 5.4.5.2, 5.5.5.2 and 5.6.5.2 for 2048 kbit/s, 8448 kbit/s, 34 368 kbit/s and 139 264 kbit/s interfaces respectively.

Output jitter should remain within the specified limits.

6.6 Input jitter and wander tolerance

6.6.1 Test specifications

The following Table lists the bit rate interfaces to be tested, together with a reference to the associated requirements clause, as applicable.

Interface (kbit/s)	Requirements Clause
2048	Clauses 5.3.7 and 5.3.5
8448	Clauses 5.4.7 and 5.4.5
34 368	Clauses 5.5.7 and 5.5.5
139 264	Clauses 5.6.7 and 5.6.5

6.6.2 Test method

The maximum tolerable jitter at the line input port should be measured using the test set-up shown in Figure 13. The bit pattern generator should be set to the appropriate interface bit rate, and generate the recommended PRBS ($2^{15} – 1$ or $2^{23} – 1$) defined in Figure 9. Jitter frequency should be varied between the minimum and the maximum limit specified, and the simulated cable loss should be varied over the stated loss range.

6.7 AIS received

The remote alarm indicator bit in time slot zero on the output port of the CE should be checked to determine that it is set when a continuous binary '1' condition (AIS) is present at the input port of the CE.

6.8 Output signal pulse shape

6.8.1 Test specifications

The following Table lists the bit rate interfaces to be tested, together with a reference to the associated requirements clause, as applicable.

Interface (kbit/s)	Requirements Clause and Figure
2048	Clause 5.3.4 and Figure 3
8448	Clause 5.4.4 and Figure 4
34 368	Clause 5.5.4 and Figure 5
139 264 Binary 0	Clause 5.6.4.1 and Figure 6
139 264 Binary 1	Clause 5.6.4.2 and Figure 7

6.8.2 Test method

The pulse at the output port loaded with its standard test load should be measured in accordance with the test set-up in Figure 10.

For a signal with HDB3 and AMI line codes, the output port of the CE should be made to transmit an isolated positive pulse followed by a space and a negative pulse followed by a space.

For a signal with CMI line code, the output port of the CE should be made to transmit long strings of 1s, and long strings of 0s.

The pulse shape should remain with in the specified limits.

6.9 Return loss

6.9.1 Test specifications

The following Table lists the bit rate interfaces to be tested, together with a reference to the associated requirements clause, as applicable.

Interface (kbit/s)	Requirements Clause
2048	Clause 5.3.5.1
8448	Clause 5.4.5.1
34 368	Clause 5.5.5.1
139 264 output port	Clause 5.6.4.1
139 264 input port	Clause 5.6.5.1

6.9.2 Test method

The input and output port return loss should be measured using the test set-up in Figure 15. The return loss bridge should use the required load impedance for the port being tested and should apply a sinusoidal test signal to the port with an amplitude as close as practical to the amplitude of the appropriate coded line signal.

The return loss of the port should be measured with the equipment powered.

6.10 Input port sensitivity

6.10.1 Test specifications

The following Table lists the bit rate interfaces to be tested, together with a reference to the associated requirements clause, as applicable.

Interface (kbit/s)	Requirements Clause
2048	Clause 5.3.5.2
8448	Clause 5.4.5.2
34 368	Clause 5.5.5.2
139 264	Clause 5.6.5.2

6.10.2 Test requirements

The input port sensitivity should be measured using the test set-up in Figure 16. No error should result with the line attenuation set to maximum and interfering signal removed.

6.11 Signal reflection immunity

6.11.1 Test specifications

The following Table lists the bit rate interfaces to be tested, together with a reference to the associated requirements clause, as applicable.

Interface (kbit/s)	Requirements Clause
2048	Clause 5.3.5.3
8448	Clause 5.4.5.3
34 368	Clause 5.5.5.3

6.11.2 Test method

The signal reflection immunity should be measured using the test set-up in Figure 16. No error should result until the interfering signal is greater than –20 dB (for 8448 kbit/s and 34 368 kbit/s) or –18 dB (for 2048 kbit/s) relative to the wanted signal.

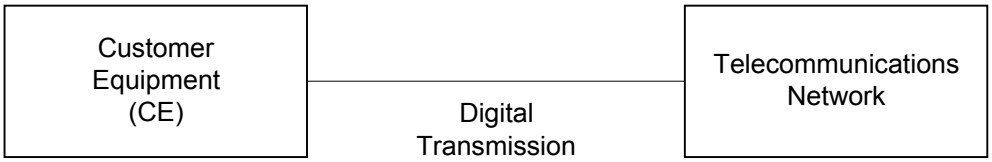


Figure 1
User-network interface reference configuration

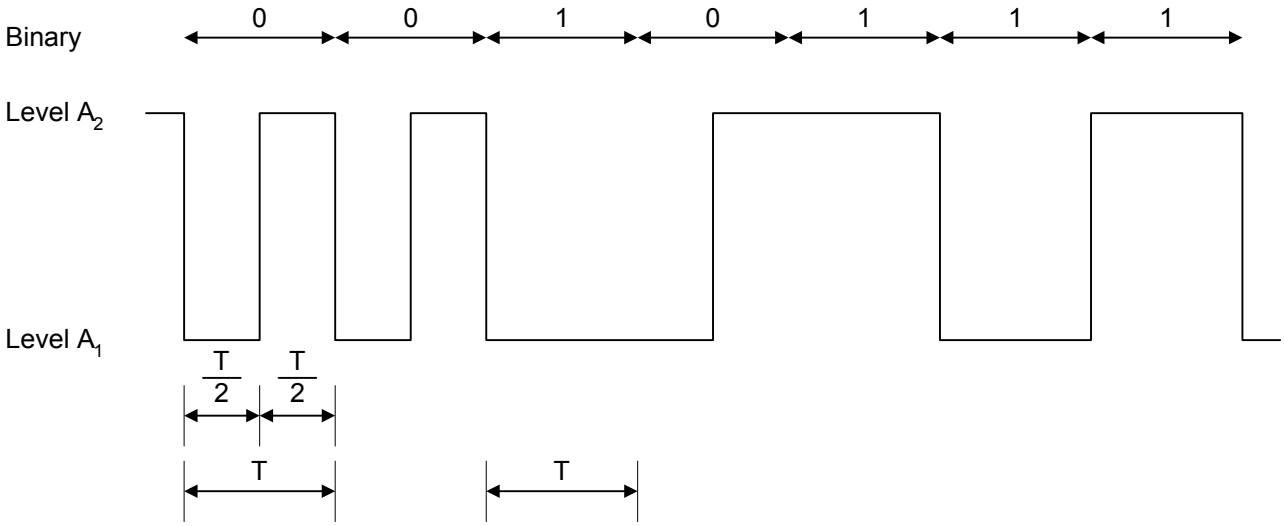
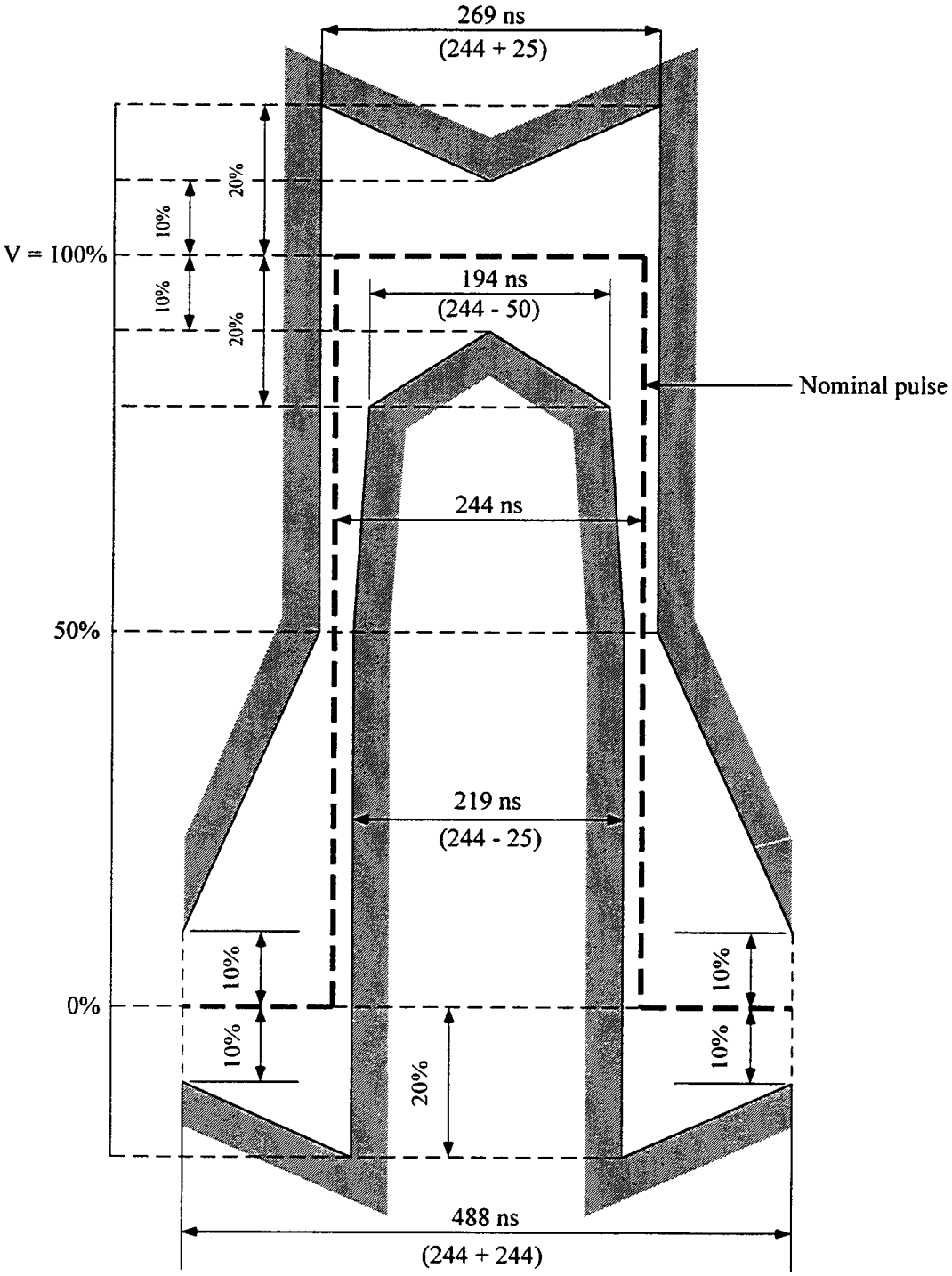


Figure 2
Example of CMI coding binary signal (informative)

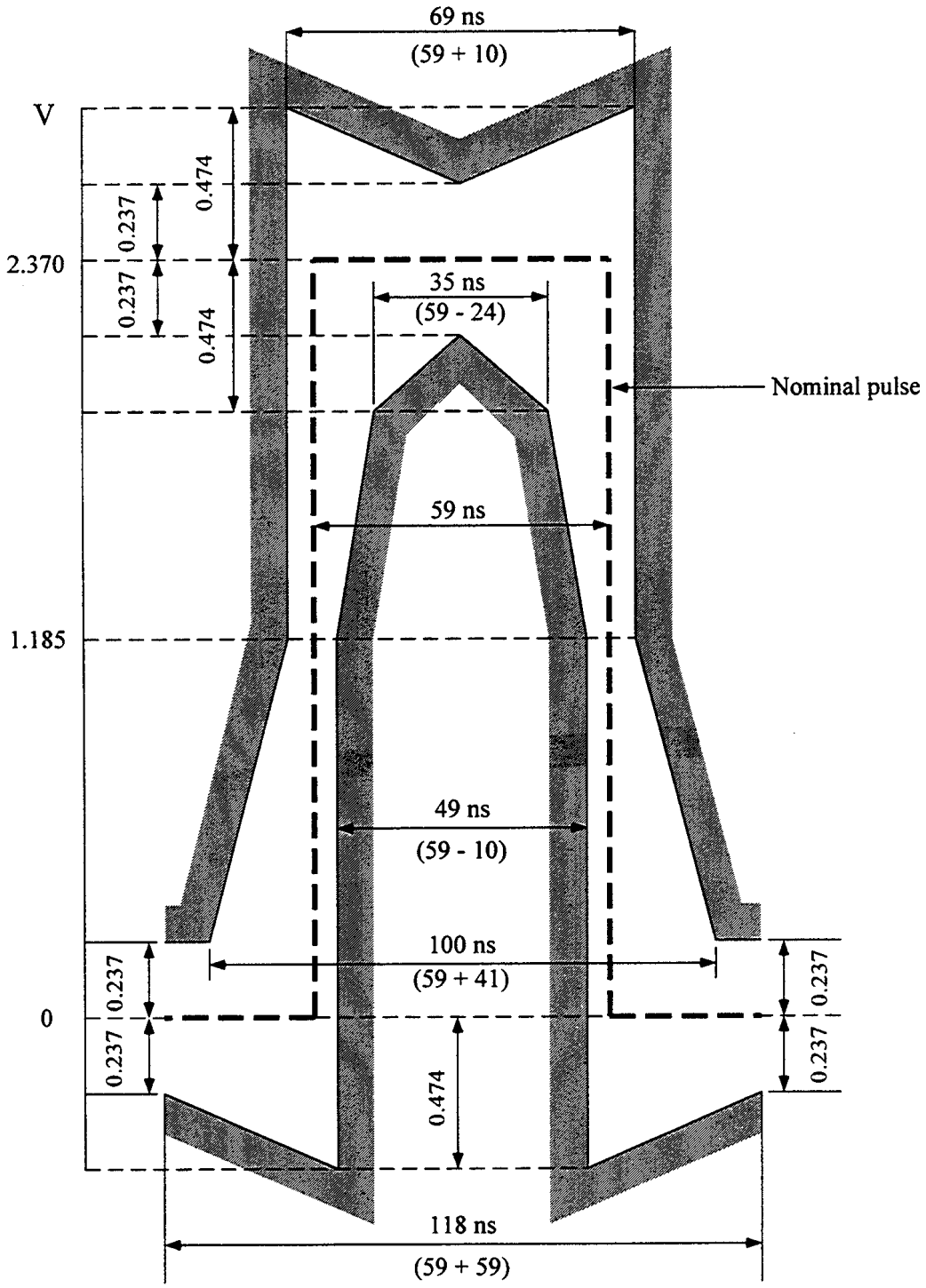


Note 1: The limits apply to pulses of either polarity.

Note 2: This mask is in accordance with Section 9 of ITU-T Rec. G.703 [3].

Figure 3

Mask of a pulse at the 2048 kbit/s interface

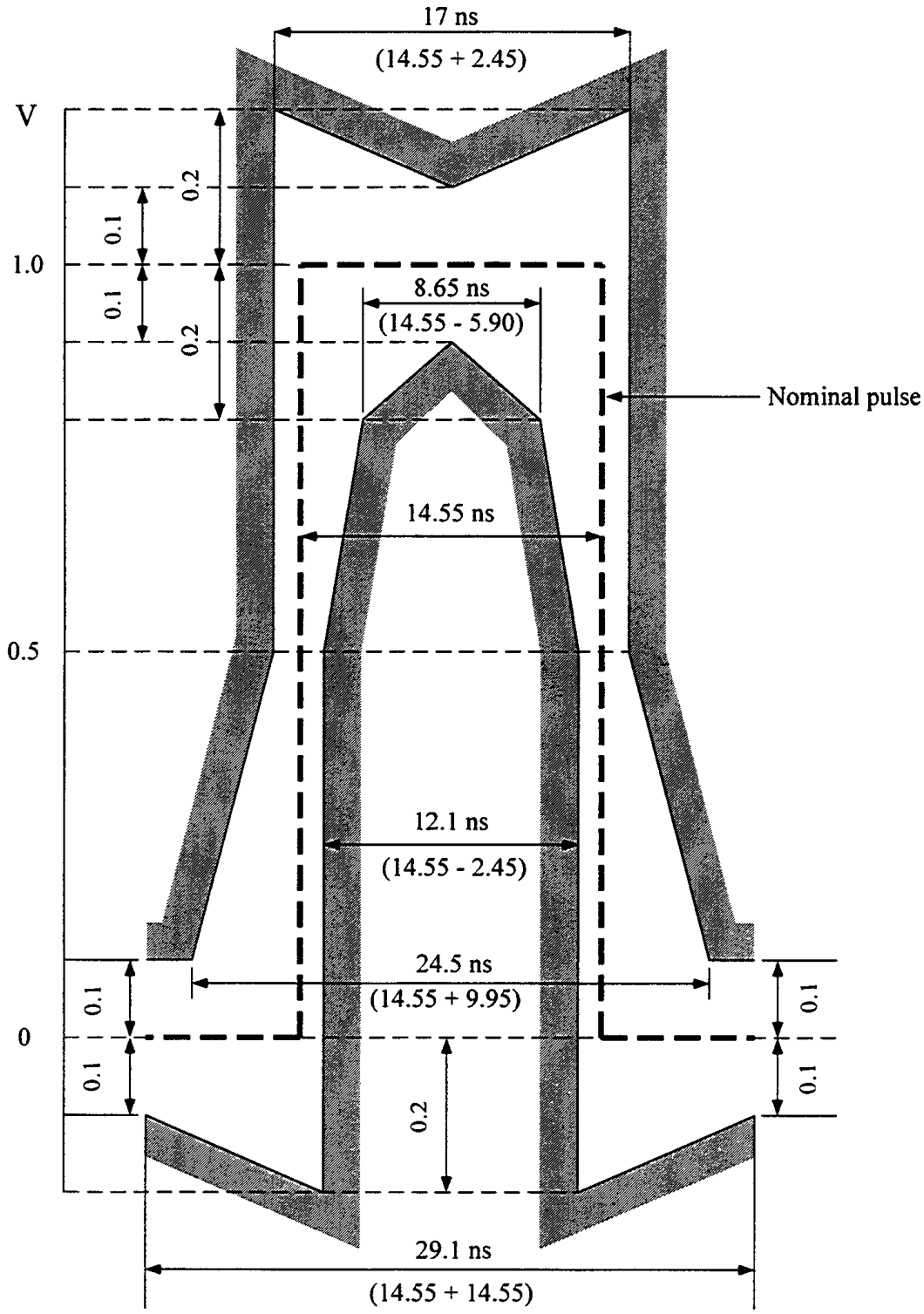


Note 1: The limits apply to pulses of either polarity.

Note 2: This mask is in accordance with Section 10 of ITU-T Rec. G.703 [3].

Figure 4

Mask of a pulse at the 8448 kbit/s interface

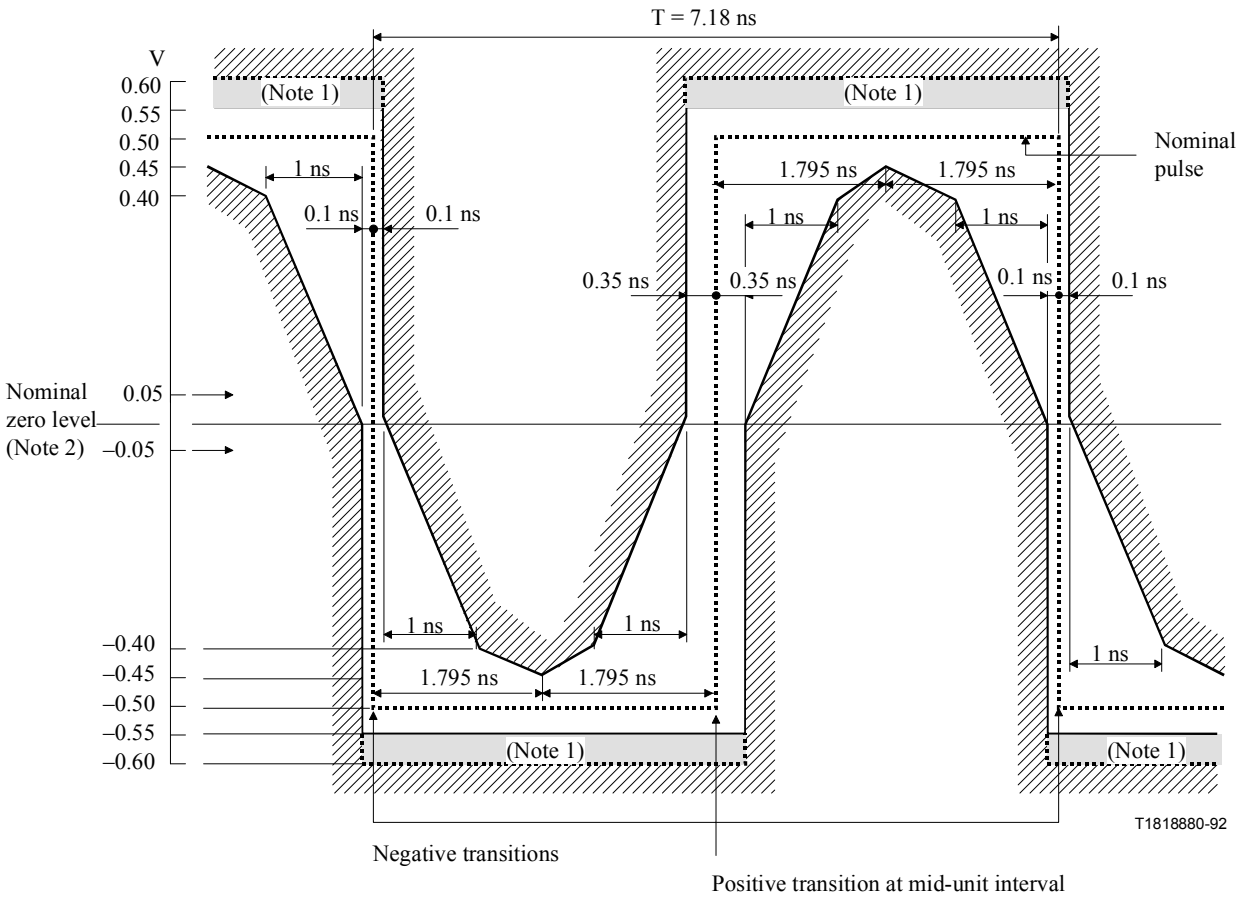


Note 1: The limits apply to pulses of either polarity.

Note 2: This mask is in accordance with Section 11 of ITU-T Rec. G.703 [3].

Figure 5

Mask of a pulse at the 34 368 kbit/s interface



Note 1: The maximum 'steady state' amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V.

Note 2: For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 μF, to the input of the oscilloscope used for measurements. The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

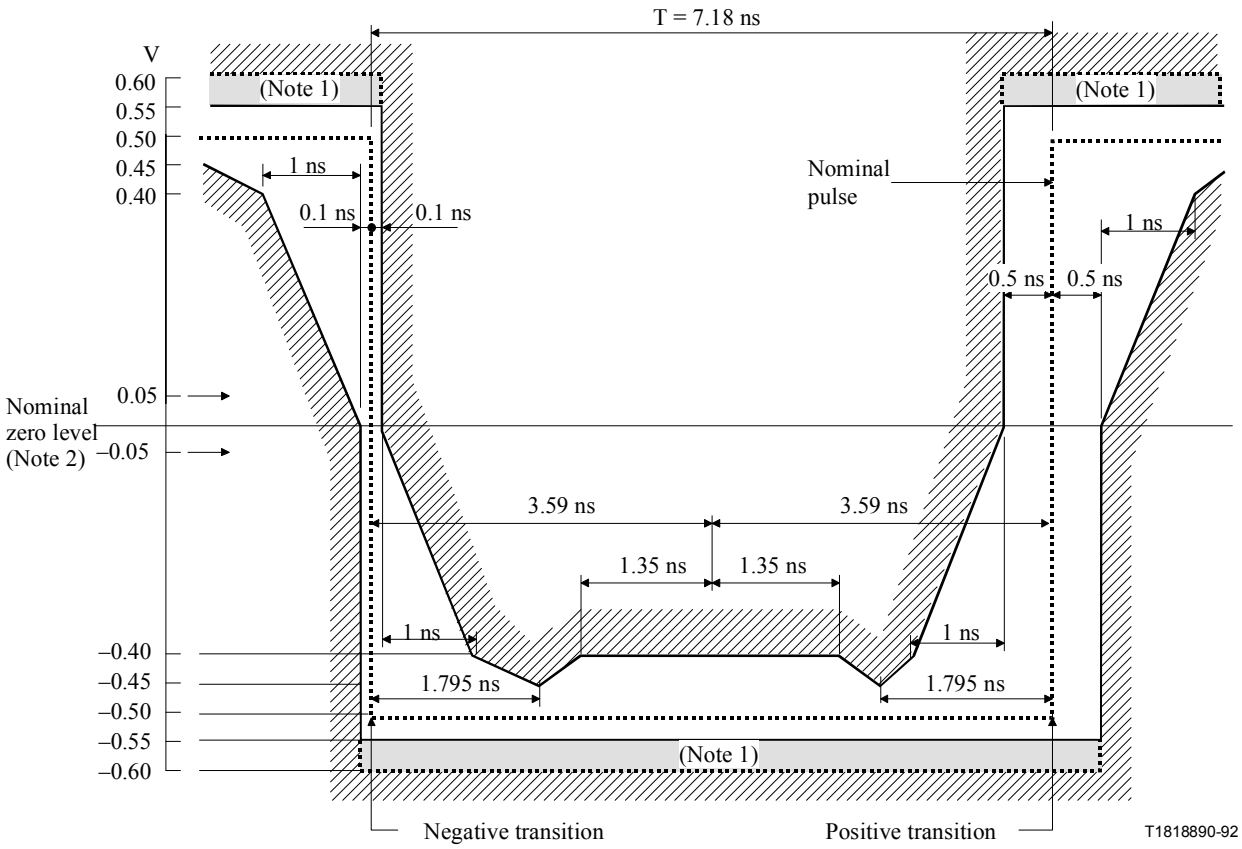
Note 3: Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their normal start and finish edges coincident. The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal. When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques (either by triggering the oscilloscope on the measured waveform or by providing both the oscilloscope and the pulse output circuits with the same clock signal).

Note 4: For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and +0.4 V, and should not exceed 2 ns.

Note 5: This mask is in accordance with Section 12 of ITU-T Rec. G.703 [3].

Figure 6

Mask of a binary 0 pulse at the 139 264 kbit/s interface



Note 1: The maximum 'steady state' amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V.

Note 2: For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 μF, to the input of the oscilloscope used for measurements. The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

Note 3: Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their normal start and finish edges coincident. The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal. When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques (either by triggering the oscilloscope on the measured waveform or by providing both the oscilloscope and the pulse output circuits with the same clock signal).

Note 4: For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and +0.4 V, and should not exceed 2 ns.

Note 5: This mask is in accordance with Section 12 of ITU-T Rec. G.703 [3].

Figure 7

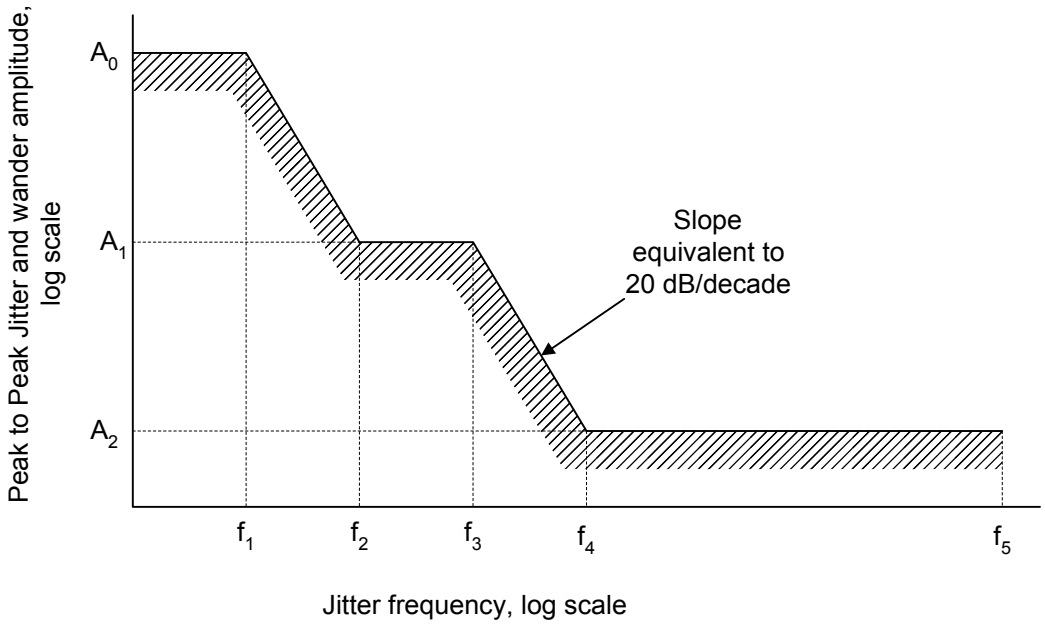
Mask of a binary 1 pulse at the 139 264 kbit/s interface

Interface	Measurement bandwidth, –3 dB frequencies (Hz)	Peak-to-peak amplitude (UI_{pp}) See Note
2048 kbit/s	20 to 100 k	1.5
	18 k to 100 k	0.2
8448 kbit/s	20 to 400 k	1.5
	3 k to 400 k	0.2
34 368 kbit/s	100 to 800 k	1.5
	10 k to 800 k	0.15
139 264 kbit/s	200 to 3.5 M	1.5
	10 k to 3.5 M	0.075

Note: For 2048 kbit/s, 1 UI = 488 ns
For 8448 kbit/s, 1 UI = 118 ns
For 34 368 kbit/s, 1 UI = 29.1 ns
For 139 264 kbit/s, 1 UI = 7.18 ns

Figure 8

Intrinsic jitter limit for output ports



Bit rate (kbits/s)	Peak to peak jitter amplitude (UI) See Note				Frequency (Hz)					PRBS test-signal
		A_1		A_2	f_1	f_2	f_3	f_4	f_5	
	f_1 to f_2	f_2 to f_3	f_3 to f_4	f_4 to f_5						
2048	30.74 / *f*	1.5	3.6×10^3 / *f*	0.2	1.67	20	2.4 k	18 k	100 k	2^{15}–1 (Rec O.151[5])
8448	N/A	1.5	600 / *f*	0.2	N/A	20	400	3 k	400 k	2^{15}–1 (Rec O.151[5])
34 368	151.2 / *f*	1.5	1.5×10^3 / *f*	0.15	4.4	100	1 k	10 k	800 k	2^{15}–1 (Rec O.151[5])
139 264	306.4 / *f*	1.5	750 / *f*	0.075	2.2	200	500	10 k	3.5 M	2^{15}–1 (Rec O.151[5])

Note: For 2048 kbits/s, 1 UI = 488 ns
For 8448 kbits/s, 1 UI = 118 ns
For 34 368 kbits/s, 1 UI = 29.1 ns
For 139 264 kbits/s, 1 UI = 7.18ns

f is in Hertz (Hz)

Figure 9

Lower limit of maximum tolerable input jitter

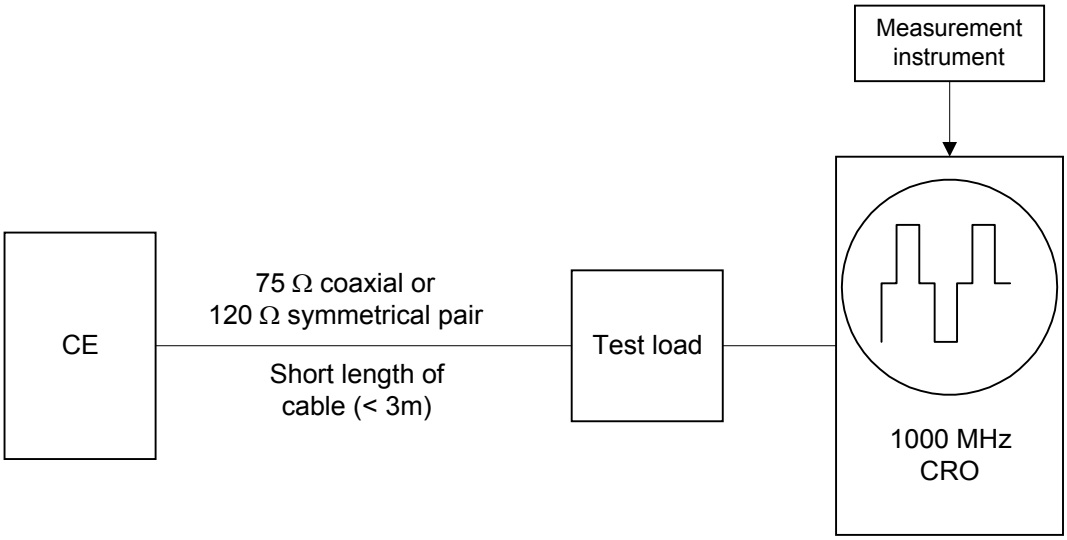


Figure 10
Output pulse shape test set-up

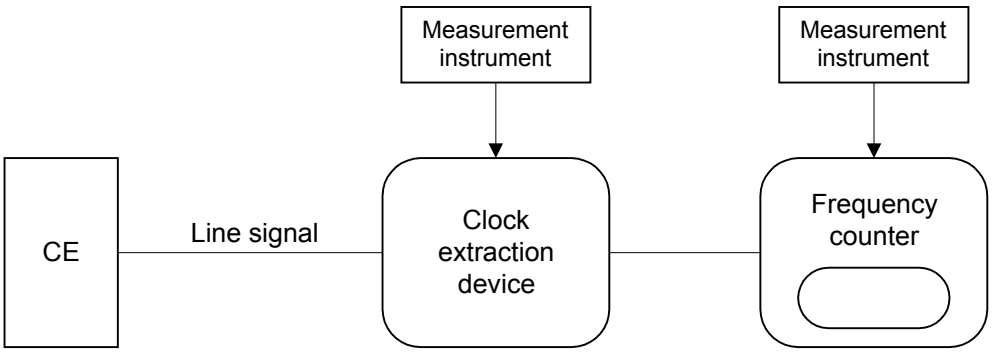


Figure 11
Bit rate and tolerance test set-up

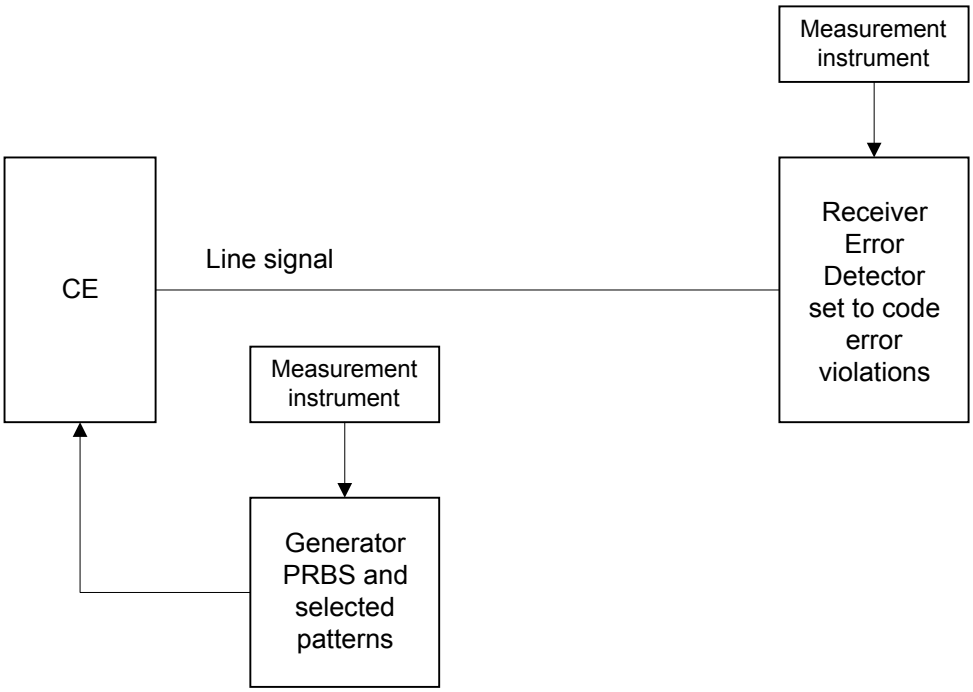


Figure 12
Line coding test set-up

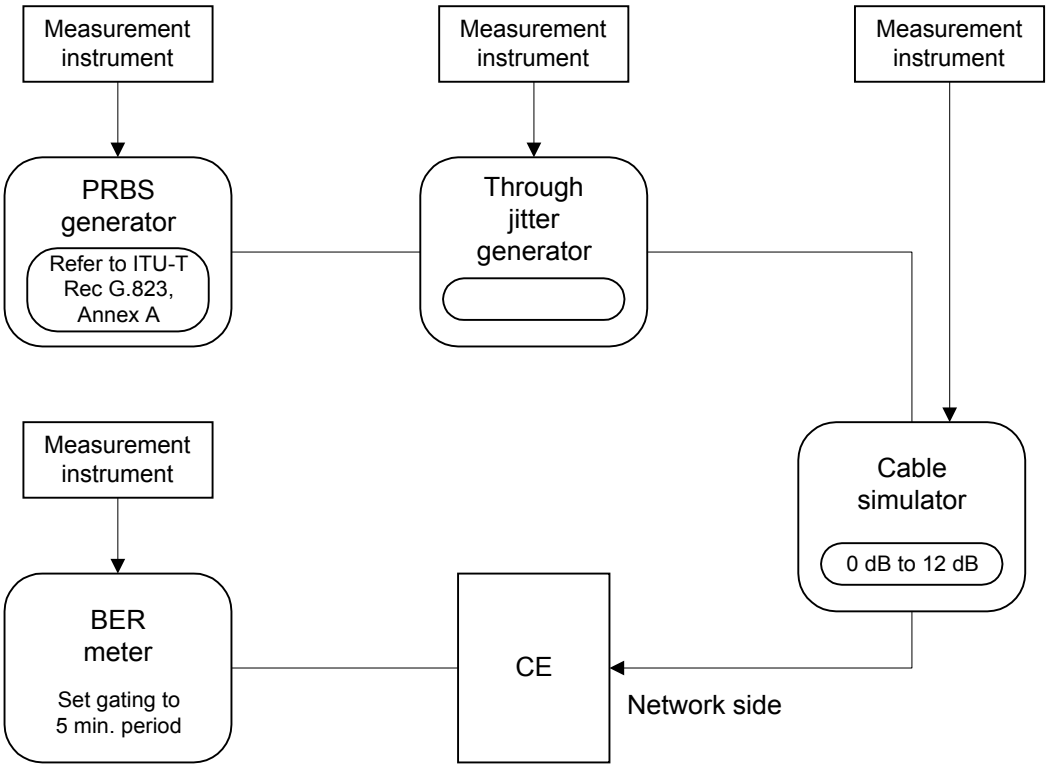


Figure 13
Input jitter and wander tolerance test set-up

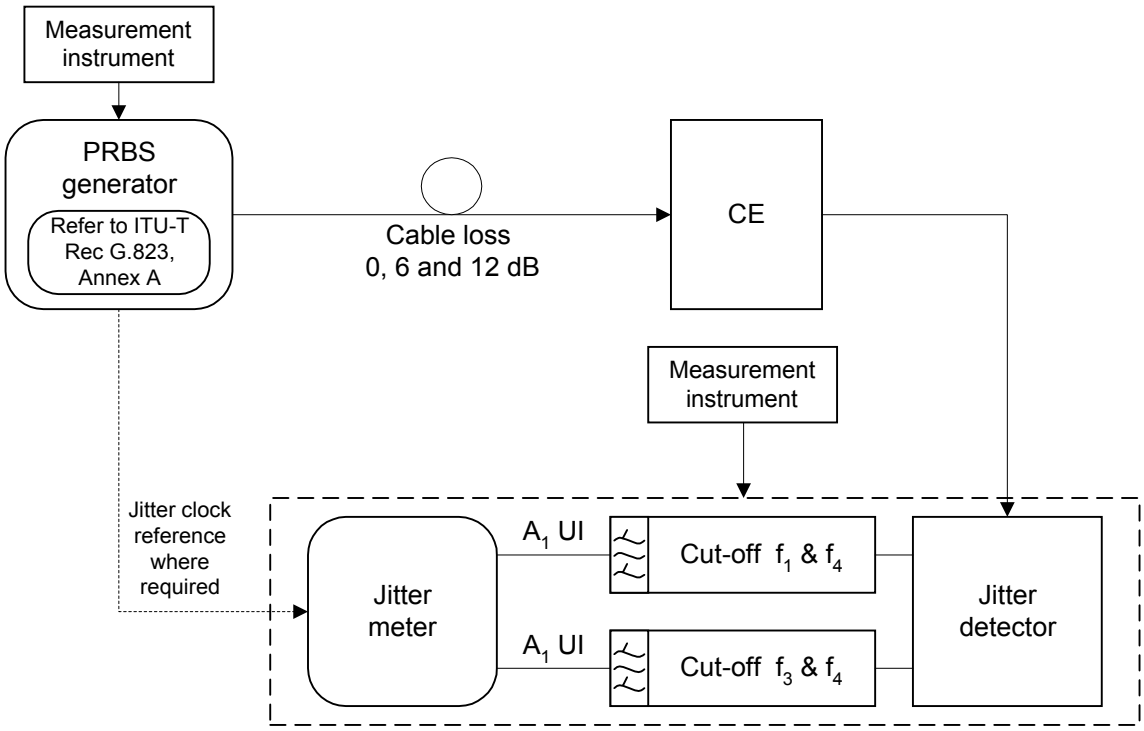
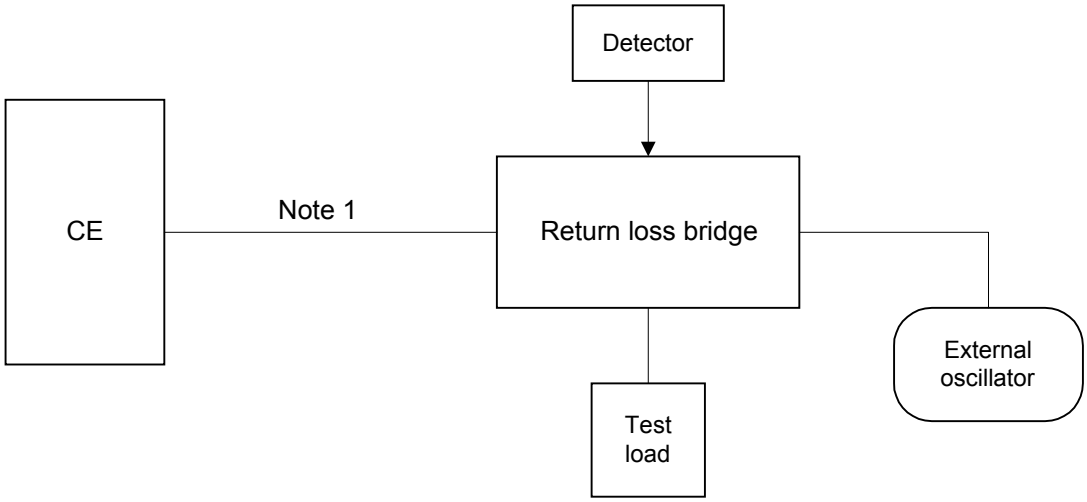


Figure 14
Intrinsic jitter test set-up



Note 1:

Bit rate (kbits/s)	Impedance (Ω)	Signal level
2048	120	3.0 V_{peak}
2048	75	2.37 V_{peak}
8448	75	2.37 V_{peak}
34 368	75	1.0 V_{peak}
139 64	75	1.0 V_{p-p}

Figure 15

Return loss test set-up

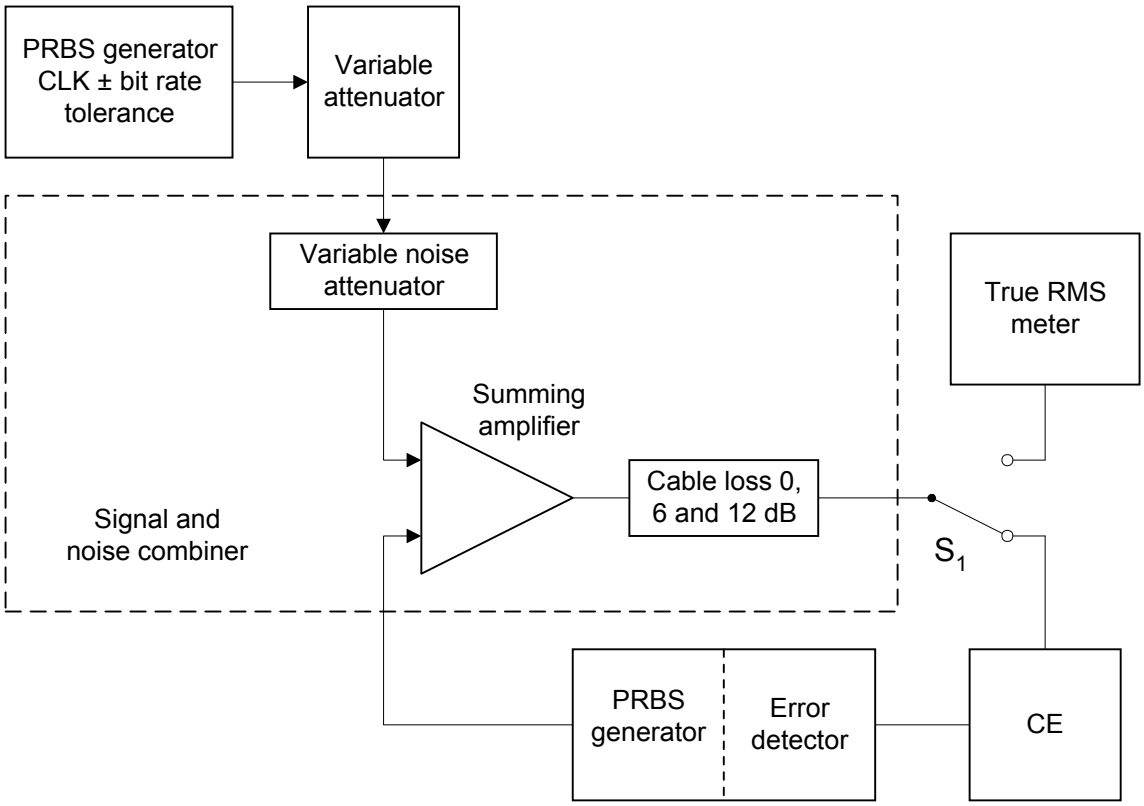


Figure 16

Signal reflection immunity test set-up

APPENDIX A
Additional recommendation for 2048 kbit/s output ports (informative)

A1 General

A.1.1 This Appendix describes an additional requirement for ensuring interoperability where output port driving circuitry allows the output impedance to vary with the line code state (B+, B–, and 0). If this variation occurs, the output pulse shape may meet the mask when loaded with the test load impedance, and yet fail to meet the mask when loaded with an input port which contains reactive components.

A.1.2 This particular form of distortion is only observed when short (e.g. 20 m or less) lengths of cable are used to connect input and output ports. As such, it may be solved by lengthening the cable, but this requirement may be avoided if the output port passes the following test. Normal practice is to provide transformers at both input and output ports, hence testing for load sensitivity is based on placing an inductor in parallel with the test load impedance.

A.1.3 The recommended specifications are as follows:

A2 75 Ω Coaxial

A.2.1 The mask of Figure 3 should be met when the output port is loaded with a 75 Ω resistor in parallel with a 100 ±5 μH inductor.

A.2.2 The load inductor should have no more than 5 Ω equivalent series winding resistance, and no less than 2700 Ω equivalent parallel eddy current and hysteresis loss resistance, when measured with a 1.7 V r.m.s. sine wave at 1 MHz.

A3 120 Ω Balanced

A.3.1 The mask of Figure 3 should be met when the output port is loaded with a 120 Ω resistor in parallel with a 160 ±8 μH inductor.

A.3.2 The load inductor should have no more than 8 Ω equivalent series winding resistance, and no less than 4320 Ω equivalent parallel eddy current and hysteresis loss resistance, when measured with a 2.1 V r.m.s. sine wave at 1 MHz.

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